# Tclok

# SAVE HOURS ON TCL/SDC/UPF

### **SCRIPT FAILURE**

# IN JUST 1 SECOND



## WHY TCLOK?

TclOK is a TCL/SDC/UPF script checking tool, featuring an innovative "static + dynamic" checking mechanism. It helps users quickly scan for basic syntax errors and other logical errors that may cause script execution to terminate before running the script.

In a large project, TCL/SDC/UPF scripts can contain thousands of lines of code and may be nested in multiple script files, making it difficult to detect hidden syntax errors. Therefore, debugging TCL/SDC/UPF scripts is challenging for design engineers, who often need to repeatedly run the scripts in the EDA tool for hours before erroring out.

TclOK can detect most errors within 1 second and provide clear descriptions and locations of the issues, allowing users to quickly resolve the script problems.

## **KEY FEATURES**

#### **Static Check**

Performs structural validation of Tcl commands, including basic syntax, argument types, and formal checks.

#### No Dependency

TclOK is not dependent on any other EDA tools. It uses initialization script to customize checking on EDAtool specific commands.

#### **Dynamic Check**

Uses virtual execution mechanism to handle native Tcl/SDC/UPF commands as well as EDA-tool specific commands.

#### **Auto Run**

Supports automatic execution of third-party programs, such as EDA tools, after successful script validation.

#### **Checking Mode**

Offers both default and verbose checking modes to facilitate different usage preferences.

#### **Script Debug**

Provides a variety of debugging methods, such as variable value printing and conditional/loop statement behavior control.

# **Contact Us**

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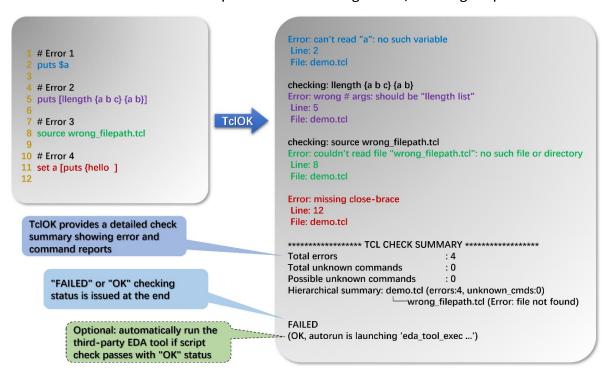
# Resources

TclOK User Guide
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### NATIVE TCL CHECKING

Native Tcl Checking quickly identifies syntax errors, command structure issues, and logical flaws in Tcl scripts. It provides detailed error summaries with precise line-level diagnostics, ensuring scripts are execution-ready.



# BUILD-IN SDC/UPF CHECKING

Built-in SDC/UPF Checking validates SDC and UPF commands. It thoroughly checks the legality of SDC/UPF command options and arguments, ensuring they meet structural and syntax requirements as well as EDA tool compatibility.

